## REMARKS

This response is intended as a full and complete response to the Office Action dated July 15, 2003. In view of the amendments and the following discussion, the Applicants believe that all claims are in allowable form.

## ELECTION OF CLAIMS

The Applicants confirm the election of claims 1-15. Claims 16-21 have been cancelled without prejudice. The Applicants reserve the right to file continuing and/or divisional applications to prosecute the non-elected subject matter.

## CLAIM REJECTIONS

**A. 35 U.S.C. §102(b) Claims 1, 2, 3, 9, and 10**

Claims 1, 2, 3, 9, and 10 stand rejected as being anticipated by United States Patent No. 6,230,069 B1 issued May 8, 2001 to Campbell et al., (hereinafter referred to as "Campbell"). In response, the Applicants have amended claims 1 and 9 to more clearly recite aspects of the invention.

Independent claims 1 and 9, as amended, recites limitations not taught, shown or suggested by Campbell. Campbell teaches a method of controlling the manufacture of semiconductor wafers using a method of model predictive control. The method uses the results of pre-polish measurements performed by a metrology tool 210 and post-polish thickness measurements performed by a metrology tool 212 to optimize time of polishing by a polishing tool 220 (col. 4, lines 8-16, FIG. 2). As such, Campbell teaches to use results of a pre-process measurement (i.e., pre-polishing thickness) taken immediately preceding a process performed in a processing tool (i.e., polishing tool 220) and a post-process measurement (i.e., post-polishing thickness) immediately following the process performed in the processing to optimize a control parameter (i.e., time). Thus, Campbell teaches to use information obtain immediately prior and subsequent to processing in single chamber to optimize control parameters within that chamber. However, Campbell does not teach, show or suggest a method of testing a workpiece (or semiconductor wafer) after a specific processing step of a plurality processing steps

performed within one or more independently operating tools, generating control parameters for at least one processing step selected from the group consisting of processing steps occurring previous to the specific processing step and processing steps occurring after a processing step subsequent to the specific processing step that is to be performed or have been performed on the workpiece (wafer) by the independently operating tools, selectively supplying said control parameters to either the previous processing steps or the subsequent processing steps, or both to optimize the processing performed upon the workpiece (wafer), as recited by claims 1 and 9, as amended.

Thus, the Applicants submit that independent claims 1 and 9, as amended, and claims 2, 3, and 10 depending therefrom, are patentable over Campbell. Accordingly, the Applicants respectfully request the rejection be withdrawn.

**B. 35 U.S.C. §103(a) Claims 4, 5, 11, and 12**

Claims 4, 5, 11, and 12 stand rejected as being unpatentable over Campbell in further view of United States Patent No. 5,966,312 issued Oct. 12, 1999 to Chen. In response, the Applicants have amended claims 1 and 9, from which claims 4, 5, 11, and 12 depend to more clearly recite aspects of the invention.

Independent claims 1 and 9, as amended, recite limitations not taught, shown or suggested by Campbell and Chen, along or in combination. The teachings of Campbell have been discussed above. Chen describes a method for monitoring and analyzing manufacturing process where statistical simulation is performed in parallel with the actual process to generate data that is indicative of the manufacturing process (col. 3, lines 15-50).

Thus, Chen cannot be utilized to modify the teachings of Campbell to yield a method a method of testing a workpiece (or semiconductor wafer) after a specific processing step of a plurality processing steps performed within one or more independently operating tools, generating control parameters for at least one processing step selected from the group consisting of processing steps occurring previous to the specific processing st p and processing steps occurring after a processing step subsequent to the specific processing step that is to be p rformed or have been

performed on the workpiece (wafer) by the independently operating tools, selectively supplying said control parameters to either the previous processing steps or the subsequent processing steps, or both to optimize the processing performed upon the workpiece (wafer), as recited by claims 1 and 9, as amended.

Thus, the Applicants submit that claims 4, 5, 11, and 12, which depend from claims 1 and 9, are patentable over Campbell in view of Chen. Accordingly, the Applicants respectfully request the rejection be withdrawn.

**C. 35 U.S.C. §103(a) Claims 6, 7, 13, and 14**

Claims 6, 7, 13, and 14 stand rejected as being unpatentable over Campbell in further view of United States Patent No. 4,411,982 issued Oct. 25, 1983 to Shibuya et al. (hereinafter referred to as "Shibuya"). In response, the Applicants have amended claim claims 1 and 9, from which claims 6, 7, 13, and 14 depend to more clearly recite aspects of the invention. Claim 13 has been amended to correct the antecedent basis for the term "tools".

Independent claims 1 and 9, as amended, recite limitations not taught, shown or suggested by Campbell and Shibuya, along or in combination. The teachings of Campbell have been discussed above. Shibuya teaches a method of making flexible printed circuit boards (workpieces). The method includes a step of retaining selected oblong parts by covering such parts with etching-resistant resin (Abstract). Although Shibuya shows multiple apparatuses for performing different process steps, Shibuya does not teach testing of a workpiece (or semiconductor wafer) after any processing steps or any criteria for generating process control parameters.

Thus, Shibuya cannot be utilized to modify the teachings of Campbell to yield a method a method of testing a workpiece (or semiconductor wafer) after a specific processing step of a plurality processing steps performed within one or more independently operating tools, generating control parameters for at least one processing step selected from the group consisting of processing steps occurring previous to the specific processing step and processing steps occurring after a processing step subsequent to the specific processing step that is to be performed or have been performed on the workpiece (wafer) by the independently operating tools, selectively

supplying said control parameters to either the previous processing steps or the subsequent processing steps, or both to optimize the processing performed upon the workpiece (wafer), as recited by claims 1 and 9, as amended.

Thus, the Applicants submit that claims 6, 7, 13, and 14, which depend from claims 1 and 9, are patentable over Campbell in view of Shibuya. Accordingly, the Applicants respectfully request the rejection be withdrawn.

**D. 35 U.S.C. §103(a) Claims 8 and 15**

Claims 8 and 15 stand rejected as being unpatentable over Campbell in further view of United States Patent No. 6,433,561 B1 issued Aug. 13, 1983 to Satya et al. (hereinafter referred to as "Satya"). In response, the Applicants have amended claims 1 and 9, from which claims 6, 7, 13, and 14 depend to more clearly recite aspects of the invention.

Independent claims 1 and 9, as amended, recite limitations not taught, shown or suggested by Campbell and Satya, along or in combination. The teachings of Campbell have been discussed above. Satya teaches a method of detecting defects is a sample (workpiece) using an optical measuring tool. Results of the measurements are processed and classified to increase probability of detecting a killer defect (col. 2, lines 33-65). Although Satya shows using sample inspection to generate automated defect classification, Satya does not teach using inspection date to generating process control parameters for at least one processing step selected from the group consisting of processing steps occurring previous to the specific processing step and processing steps occurring after a processing step subsequent to the specific processing step that is to be performed or have been performed on the workpiece (wafer) by a independently operating tools that process the workpiece (wafer).

Thus, Satya cannot be utilized to modify the teachings of Campbell to yield a method a method of testing a workpiece (or semiconductor wafer) after a specific processing step of a plurality processing steps performed within one or more independently operating tools, generating control parameters for at least one processing step select d from the group consisting of processing st ps occurring previous to the specific processing step and processing steps occurring after a processing step

subsequent to the specific processing step that is to be performed or have been performed on the workpiece (wafer) by the independently operating tools, selectively supplying said control parameters to either the previous processing steps or the subsequent processing steps, or both to optimize the processing performed upon the workpiece (wafer), as recited by claims 1 and 9, as amended.

Thus, the Applicants submit that claims 8 and 15, which depend from claims 1 and 9, are patentable over Campbell in view of Satya. Accordingly, the Applicants respectfully request the rejection be withdrawn.

## CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Keith Taboada at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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